central area, because of a distribution of a pressure applied to the wafer, a distribution of a slurry supply amount and the like. There is, therefore, a tendency that the second insulating layer 18 after CMP is thick in the wafer central area and thin in the wafer peripheral area.

The paragraph beginning at line 14, page 15, has been rewritten as follows:

Fig. 1D is a plane view of the wafer 1 . In the effective wafer area indicated by hatched lines, hole patterns are formed, whereas in the peripheral wafer area around the effective wafer area, hole patterns are not formed. Since hole patterns are not formed in the peripheral wafer area, it is possible to prevent the second etching stopper layer 17 from being etched and the main wiring payer 16 from being oxidized and decomposed.

The paragraph beginning at line 16, page 21, has been rewritten as follows:

As shown in Fig. 3B, on the semiconductor wafer formed with wiring grooves and conductor grooves, a first barrier metal layer 15 and a first main wiring layer 16 are formed. For example, the barrier metal layer 15 is made of a Ta layer of 50 nm thick, and the main wiring layer 16 is made of a Cu layer of 1500 nm. Thereafter, CMP is performed to remove unnecessary regions of the main wiring layer 16 and barrier metal layer 15 on the surface of the silicon oxide layer 42.

The paragraph beginning at line 19, page 24, has been rewritten as follows:

On an active region defined by STI, an insulated gate electrode 5 and a side wall spacer 6 are formed, and on both sides of the gate electrode, source/drain regions S/D are formed through ion

implantation. A first etching stopper layer s1 is formed covering the insulated gate electrode, and a first lower insulating layer da1 is formed on the first etching stopper layer s1. A conductive plug is formed through the first lower insulating layer da1 and first etching stopper layer s1, the conductive plug being constituted on a barrier metal layer 7 and a wiring metal region 8.

The paragraph beginning at line 4, page 27, has been rewritten as follows:

As shown in Fig. 5A, on an underlying structure 111, an organic insulating film 112 made of, for example, SiLK, is coated to a thickness of 250nm. For example, the underlying structure 111 is a structure that conductive plugs are embedded in the first lower insulating layer da1 shown in Fig. 4. Conductive plugs 110 are not formed in the wafer edge area. Coated material in the peripheral wafer area is removed by rinsing using etchant by about 3mm +- 0.5mm from the wafer edge. Next, an insulating film 113 made of, for example, a silicon oxide film of about 250 nm thick, is deposited by CVD to cover the whole surface of the organic insulating layer 112.

The paragraph beginning at line 13, page 39, has been rewritten as follows:

As shown in Fig. 9L, the wiring layer 25 is polished by CMP from its surface to remove unnecessary regions of the wiring layer 25 and metal layer 47. In this case, in the wafer edge area, polishing is stopped in the state that the wiring layer 25 covers the side wall of the organic insulating layer 45. An etching stopper layer 26 made of, for example, an SiN layer of 50 nm thick or a surface protective layer is formed covering the surface of the wiring layer 25.